

7 x 5 x 1.8mm 6 pad SMD





Frequency range 0.625MHz to 50.0MHz

CMOS/TTL Output

- Supply Voltage 5.0 V or 3.3 VDC
- **Integrated Phase Jitter 1ps typical**
- Low cost unit

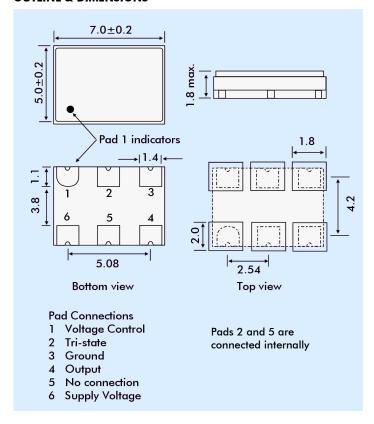
DESCRIPTION

G576 VCXOs, are packaged in a miniature 7mm x 5mm x 1.8mm 6 pad SMD package. Typical phase jitter for G series VCXOs is <1ps, output CMOS/TTL. G series VCXOs use fundamental mode crystal osccillators. Applications include phase lock loop, SONET/ATM, settop boxes, MPEG, audio/video modulation, video game consoles and HDTV.

SPECIFICATION

Frequency Range			
Vdd = +3.3VDC:	0.625MHz to 50.0MHz		
Vdd = +5.0VDC:	1.0MHz to 50.0MHz		
Supply Voltage:	+3.3 VDC ±5% or +5.0VDC±5%		
Output Logic:	TTL/HCMOS		
Integrated Phase Jitter:	1.0ps maximum 12kHz to 20MHz		
Period Jitter RMS:	2.0ps typical		
Period Jitter Peak to Peak:	14ps maximum		
Phase Noise:	See table below		
Initial Frequency Accuracy			
Tune to the nominal frequency wi	th:		
+3.3VDC:	$Vc = 1.65V \pm 0.2V$		
+5.0 VDC:	$Vc = 2.5V \pm 0.2V$		
Output Voltage HIGH (1):	90% Vdd minimum		
Output Voltage LOW (0):	10% Vdd maximum		
Control Voltage Centre			
+3.3VDC:	1.65V		
+5.0VDC:	2.5V		
Control Voltage Range			
+3.3VDC:	0.3V to 3.0V		
+5.0VDC:	0.5V to 4.5V		
+3.0VDC:			
	0.57 10 4.57		
Pulling Range			
Pulling Range +3.3VDC	±80ppm to ±120ppm (standard)		
Pulling Range	±80ppm to ±120ppm (standard) ±80ppm to ±150ppm		
Pulling Range +3.3VDC +5.0VDC:	±80ppm to ±120ppm (standard) ±80ppm to ±150ppm (±200ppm available)		
Pulling Range +3.3VDC +5.0VDC: Temperature Stability:	±80ppm to ±120ppm (standard) ±80ppm to ±150ppm (±200ppm available) See table		
Pulling Range +3.3VDC +5.0VDC: Temperature Stability: Output Load:	±80ppm to ±120ppm (standard) ±80ppm to ±150ppm (±200ppm available) See table CMOS = 15pF, TTL = 2 gates		
Pulling Range +3.3VDC +5.0VDC: Temperature Stability: Output Load: Start-up Time:	±80ppm to ±120ppm (standard) ±80ppm to ±150ppm (±200ppm available) See table CMOS = 15pF, TTL = 2 gates 10ms maximum, 5ms typical		
Pulling Range +3.3VDC +5.0VDC: Temperature Stability: Output Load: Start-up Time: Duty Cycle:	±80ppm to ±120ppm (standard) ±80ppm to ±150ppm (±200ppm available) See table CMOS = 15pF, TTL = 2 gates 10ms maximum, 5ms typical 50% ±5% measured at 50% Vdd		
Pulling Range +3.3VDC +5.0VDC: Temperature Stability: Output Load: Start-up Time: Duty Cycle: Rise/Fall Times:	±80ppm to ±120ppm (standard) ±80ppm to ±150ppm (±200ppm available) See table CMOS = 15pF, TTL = 2 gates 10ms maximum, 5ms typical 50% ±5% measured at 50% Vdd 0.7ns typical (15pF load)		
Pulling Range +3.3VDC +5.0VDC: Temperature Stability: Output Load: Start-up Time: Duty Cycle:	±80ppm to ±120ppm (standard) ±80ppm to ±150ppm (±200ppm available) See table CMOS = 15pF, TTL = 2 gates 10ms maximum, 5ms typical 50% ±5% measured at 50% Vdd 0.7ns typical (15pF load) 10 to 45mA, frequency		
Pulling Range +3.3VDC +5.0VDC: Temperature Stability: Output Load: Start-up Time: Duty Cycle: Rise/Fall Times: Current Consumption:	±80ppm to ±120ppm (standard) ±80ppm to ±150ppm (±200ppm available) See table CMOS = 15pF, TTL = 2 gates 10ms maximum, 5ms typical 50% ±5% measured at 50% Vdd 0.7ns typical (15pF load) 10 to 45mA, frequency dependent		
Pulling Range +3.3VDC +5.0VDC: Temperature Stability: Output Load: Start-up Time: Duty Cycle: Rise/Fall Times: Current Consumption: Linearity:	±80ppm to ±120ppm (standard) ±80ppm to ±150ppm (±200ppm available) See table CMOS = 15pF, TTL = 2 gates 10ms maximum, 5ms typical 50% ±5% measured at 50% Vdd 0.7ns typical (15pF load) 10 to 45mA, frequency dependent 10% maximum, 6% typical		
Pulling Range +3.3VDC +5.0VDC: Temperature Stability: Output Load: Start-up Time: Duty Cycle: Rise/Fall Times: Current Consumption: Linearity: Modulation Bandwidth:	±80ppm to ±120ppm (standard) ±80ppm to ±150ppm (±200ppm available) See table CMOS = 15pF, TTL = 2 gates 10ms maximum, 5ms typical 50% ±5% measured at 50% Vdd 0.7ns typical (15pF load) 10 to 45mA, frequency dependent 10% maximum, 6% typical 10kHz minimum		
Pulling Range +3.3VDC +5.0VDC: Temperature Stability: Output Load: Start-up Time: Duty Cycle: Rise/Fall Times: Current Consumption: Linearity: Modulation Bandwidth: Input Impedance:	±80ppm to ±120ppm (standard) ±80ppm to ±150ppm (±200ppm available) See table CMOS = 15pF, TTL = 2 gates 10ms maximum, 5ms typical 50% ±5% measured at 50% Vdd 0.7ns typical (15pF load) 10 to 45mA, frequency dependent 10% maximum, 6% typical 10kHz minimum 1 MΩ minimum		
Pulling Range +3.3VDC +5.0VDC: Temperature Stability: Output Load: Start-up Time: Duty Cycle: Rise/Fall Times: Current Consumption: Linearity: Modulation Bandwidth: Input Impedance: Slope Polarity:	±80ppm to ±120ppm (standard) ±80ppm to ±150ppm (±200ppm available) See table CMOS = 15pF, TTL = 2 gates 10ms maximum, 5ms typical 50% ±5% measured at 50% Vdd 0.7ns typical (15pF load) 10 to 45mA, frequency dependent 10% maximum, 6% typical 10kHz minimum 1 MΩ minimum Monotonic and Positive. (An		
Pulling Range +3.3VDC +5.0VDC: Temperature Stability: Output Load: Start-up Time: Duty Cycle: Rise/Fall Times: Current Consumption: Linearity: Modulation Bandwidth: Input Impedance:	±80ppm to ±120ppm (standard) ±80ppm to ±150ppm (±200ppm available) See table CMOS = 15pF, TTL = 2 gates 10ms maximum, 5ms typical 50% ±5% measured at 50% Vdd 0.7ns typical (15pF load) 10 to 45mA, frequency dependent 10% maximum, 6% typical 10kHz minimum 1 MΩ minimum Monotonic and Positive. (An increase of control voltage		
Pulling Range +3.3VDC +5.0VDC: Temperature Stability: Output Load: Start-up Time: Duty Cycle: Rise/Fall Times: Current Consumption: Linearity: Modulation Bandwidth: Input Impedance: Slope Polarity:	±80ppm to ±120ppm (standard) ±80ppm to ±150ppm (±200ppm available) See table CMOS = 15pF, TTL = 2 gates 10ms maximum, 5ms typical 50% ±5% measured at 50% Vdd 0.7ns typical (15pF load) 10 to 45mA, frequency dependent 10% maximum, 6% typical 10kHz minimum 1 MΩ minimum Monotonic and Positive. (An increase of control voltage always increases output		
Pulling Range +3.3VDC +5.0VDC: Temperature Stability: Output Load: Start-up Time: Duty Cycle: Rise/Fall Times: Current Consumption: Linearity: Modulation Bandwidth: Input Impedance: Slope Polarity: (Transfer function)	±80ppm to ±120ppm (standard) ±80ppm to ±150ppm (±200ppm available) See table CMOS = 15pF, TTL = 2 gates 10ms maximum, 5ms typical 50% ±5% measured at 50% Vdd 0.7ns typical (15pF load) 10 to 45mA, frequency dependent 10% maximum, 6% typical 10kHz minimum 1 MΩ minimum Monotonic and Positive. (An increase of control voltage always increases output frequency.)		
Pulling Range +3.3VDC +5.0VDC: Temperature Stability: Output Load: Start-up Time: Duty Cycle: Rise/Fall Times: Current Consumption: Linearity: Modulation Bandwidth: Input Impedance: Slope Polarity: (Transfer function) Storage Temperature:	±80ppm to ±120ppm (standard) ±80ppm to ±150ppm (±200ppm available) See table CMOS = 15pF, TTL = 2 gates 10ms maximum, 5ms typical 50% ±5% measured at 50% Vdd 0.7ns typical (15pF load) 10 to 45mA, frequency dependent 10% maximum, 6% typical 10kHz minimum 1 M\O minimum Monotonic and Positive. (An increase of control voltage always increases output frequency.) -50° to +100°C		
Pulling Range +3.3VDC +5.0VDC: Temperature Stability: Output Load: Start-up Time: Duty Cycle: Rise/Fall Times: Current Consumption: Linearity: Modulation Bandwidth: Input Impedance: Slope Polarity: (Transfer function)	±80ppm to ±120ppm (standard) ±80ppm to ±150ppm (±200ppm available) See table CMOS = 15pF, TTL = 2 gates 10ms maximum, 5ms typical 50% ±5% measured at 50% Vdd 0.7ns typical (15pF load) 10 to 45mA, frequency dependent 10% maximum, 6% typical 10kHz minimum 1 MΩ minimum Monotonic and Positive. (An increase of control voltage always increases output frequency.)		

OUTLINE & DIMENSIONS



PART NUMBERING

В

С

D

Ε

FREQUENCY STABILITY

PART NUMBERING			
	Example: 3G	576 <mark>B</mark> -8	<u>0N-27.000</u>
Supply Voltage 3 = +3.3V 5 = +5.0V Series Designator G576 Stability over temperatu (See table) Pullability in ±ppm Pullability determinator N = minimum M = maximum T = Typical	,		
Frequency in MHz			

Stability Code | Stability ±ppm | Temp. Range 25

50

25 50

100

100

If non-standard frequency stability is required Use 'I' followed by stability, i.e. I20 for ±20ppm

0°~+70°C

0°~+70°C 0°~+70°C

-40°~+85°C

-40°~+85°C

-40°~+85°C

PHASE NOISE

Offset	Frequency 27.0MHz	
10Hz	-70dBc/Hz	
100Hz	-105dBc/Hz	
1kHz	-132dBc/Hz	
10kHz	-142dBc/Hz	
1MHz	-150dBc/Hz	